THALES
Building a future we can all trust

RISC-V et open-source hardware
Point de vue d'un industriel

Sécurité et Architecture RISC-V
Campus Cyber
16 mai 2024

www.thalesgroup.com

Intervenants Thales aujourd’hui

> Jérôme Quévremont

> RISC-V and open hardware project leader

> Thales Research & Technology

> Jean-Roch Coulon

> RISC-V processor architect

> Thales DIS / Thales Secure Silicon

> Emmanuel Gureghian

> Responsable du laboratoire systèmes embarqués critiques

> Thales Research & Technology

Motivation

RISC-V, open hardware

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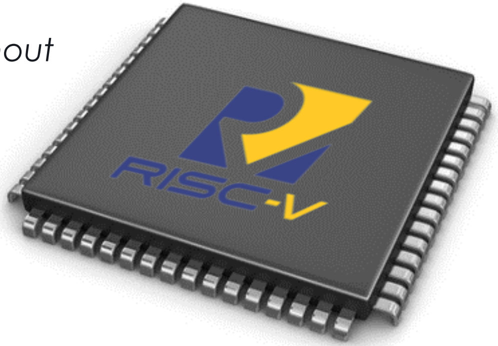
Why Thales invests in RISC-V (and open-source HW)?

Differentiator
Enabler

Share cost instead of purchasing IP
Open-source community

Security
A fully auditable processor

Sovereignty
Possible commercial exploitation without export constraints
Enable strong EU investment



No vendor-locking
Business opportunities for support, customization…

Safety
No black-box

Software
Large ecosystem compatible across implementations

SWaP & customization
Exact fit between features and application needs

Performance
State-of-the-art processor

Thales member of the OpenHW Group and RISC-V International

Our RISC-V communities

RISC-V International ("the Foundation")

- Specifies the open **RISC-V instruction set**
  - ✓ Simple & modular
  - ✓ 32- or 64-bit
  - ✓ Custom extensions
  - ✓ Covers a wide range of needs, **from MCU to HPC**
- Currently specifying **upcoming optional extensions**
- Hosts several **special interest groups** (SIG)
- Does not deliver implementations

OpenHW Group

- **Not-for-profit corporation** steered by its members
- Goal: deliver **open-source IP for production SoCs**
  - ✓ RISC-V compatible cores
  - ✓ SoC IP blocks
  - ✓ Verification environment
  - ✓ Supporting SW and tools
- Permissive, open-source, export-friendly **license**

CVA6 core

RISC-V and OpenHW

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CVA6 ecosystem

OPENHW GROUP — PROVEN PROCESSOR IP

- Thales leads the CVA6 core project at the OpenHW Group
- Over four years, a vivid ecosystem has expanded around CVA6, with several OpenHW projects

CVA6 OpenHW+TRISTAN workshop, January 2024

Contributors to CVA6 OpenHW ecosystem

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10x ENGINEERS

MU ELECTRONICS

Universidade do Minho

PlanV

OPENHW GROUP

AXELERA ARTIFICIAL INTELLIGENCE

UC SANTA BARBARA

ALMA MATER STUDIORUM UNIVERSITÀ DI BOLOGNA

ETH zürich

cea

KALRAY THE POWER OF MORE

BOSCH

POLYTECHNIQUE MONTRÉAL

Red Hat

Empaiot.

Rumble Development

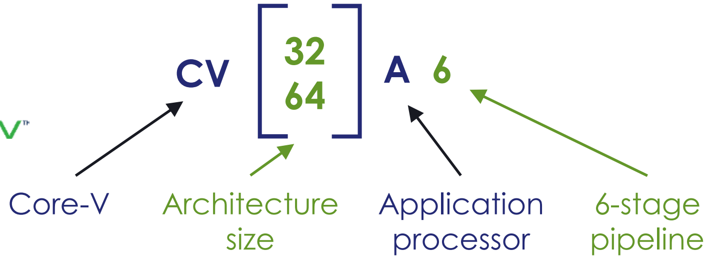
CVA6 core

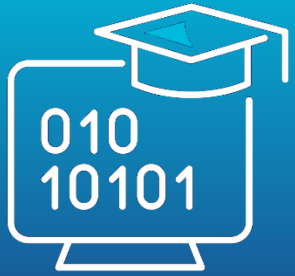
> Open-source RISC-V application core

- Supports rich OSes like Linux

> Common source code, two flavors:

- CV64A6
  - 64-bit
  - ARIANE donated by ETH Zürich to OpenHW
- CV32A6
  - 32-bit
  - Compact version designed by Thales





An academic project turning into an industrial-grade CPU core

CVA6 architecture

- > **Fully compatible with the RISC-V open ISA**
- > **6-stage pipeline, single issue, branch prediction**
  - Soon dual-issue
- > **L1 data and instruction caches**
- > **AXI4 interfaces**
- > **M/S/U/H privileges**
- > **Safe and secure features**
  - More upcoming (SECDED, DCLS)
- > **MMU and memory protection**
- > **Ready for multi/many-core CPUs**
  - e.g. open-source OpenPiton framework

A 6-stage application CPU

Different cores, one solution

- 32/64 bit
- MMU / baremetal
- Floating-point: none, SP or DP
- Optional PMP (physical memory protection)
- Optional H (hypervisor) privilege mode
- Configurable L1 caches
  - Write-through/write-back
  - Size and number of ways
- Optional coprocessor interface (CV-X-IF)
- Design optimizations
  - ASIC/FPGA
- Other options
  - C, A, Zb* extensions
  - Generic performance counters
  - Bit extension on AXI (failure protection…)

Configure CVA6 for your application and constraints, either on ASIC and FPGA

All configurations are RISC-V compatible and supported by GCC

An extendable core

> CV-X-IF interface to extend the CVA6 instruction set

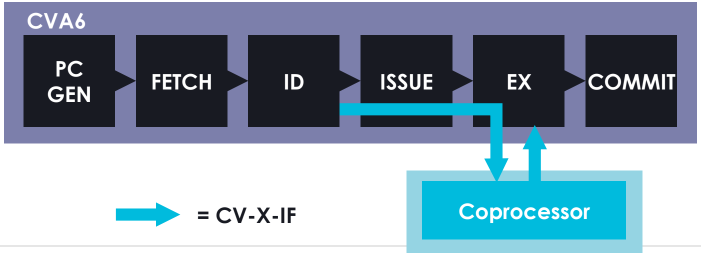
- Current or future RISC-V extensions (B, P…)
- Custom extensions (crypto, DSP, AI…)

> CV-X-IF specified by OpenHW Group

- Open specification, can be used off OpenHW
- Reuse coprocessors between CORE-V cores (CVA6, CV32E40X, CVE2)

> Compiler support

- Seamless for RISC-V standard extensions (e.g. B)
- LLVM should ease the support of custom extensions
- Inline ASM possible for specific processing



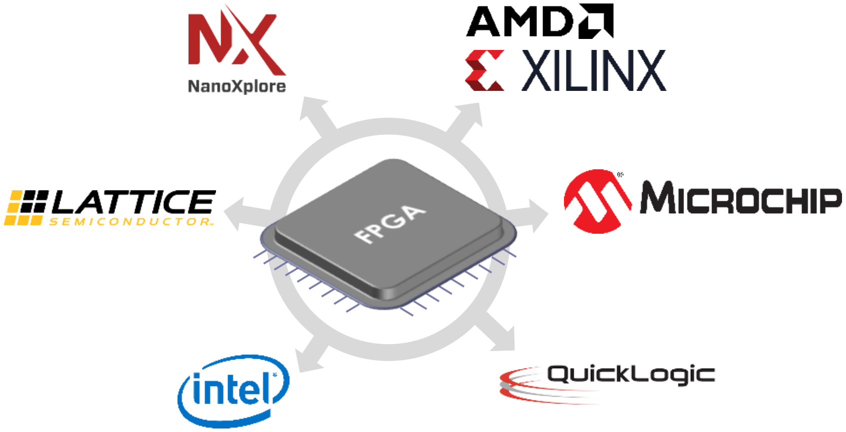
Speed up your application with a custom accelerator

Add extensions without fully re-validating the core

Multi-sourcing

> For ASIC targets (32/64 bit)

> For any FPGAs (32 bit)



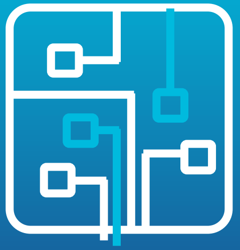
Leverage your investment: reuse your HW/SW architectures throughout your product range

(multi-sourcing: any ASIC and FPGA vendors)

HW implementations

CV32A6	FPGA			
Frequency	189 MHz			
Performance	2.8 CoreMark/MHz 530 CoreMark			
Resources	8,108 LUT	4,534 FF	12 BRAM	4 DSP
Technology	Zynq UltraScale+ -3			
Configuration	RV32IMA, 8K D$ + 8K I$, noFPU, MMU			

CV32A6	ASIC
Frequency	900 MHz
Performance	3.09 CoreMark/MHz 2781 CoreMark
Resources	80 kgates
Technology	28 nm (worst case corner)
Configuration	RV32IMA, 8K I$ + no D$, noFPU, noMMU



Upcoming dual issue
+50% perf / cycle

SW ecosystem

Boot and FW

- **U-Boot**
- **OpenSBI**

OS support

- **Linux:** 32 & 64 bit
- **Yocto** honister, **Buildroot** 2021.08
- **FreeRTOS:** 32 & 64 bit
- **RTEMS** 6
- CVA6 compatible with many others

Compiler

- Standard **GCC 13** (previously 11.2)
- Libraries: **glibc** (2.70), Newlib (4.3.0)…
- CLANG/LLVM 16, **RUST**

Debug

- HW and baremetal: JTAG probe, OpenOCD, **GDB 13**/Eclipse IDE
- Linux-based: GDB server

Full open-source software ecosystem

Protect your HW investments

Lessons learnt from open-sourcing

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What is Open-Source ?

Development strategy:
Roadmap

Specifications

Technical melting pot:
OpenHWgroup meetings,
multi organizations

Source code :
RTL, C code

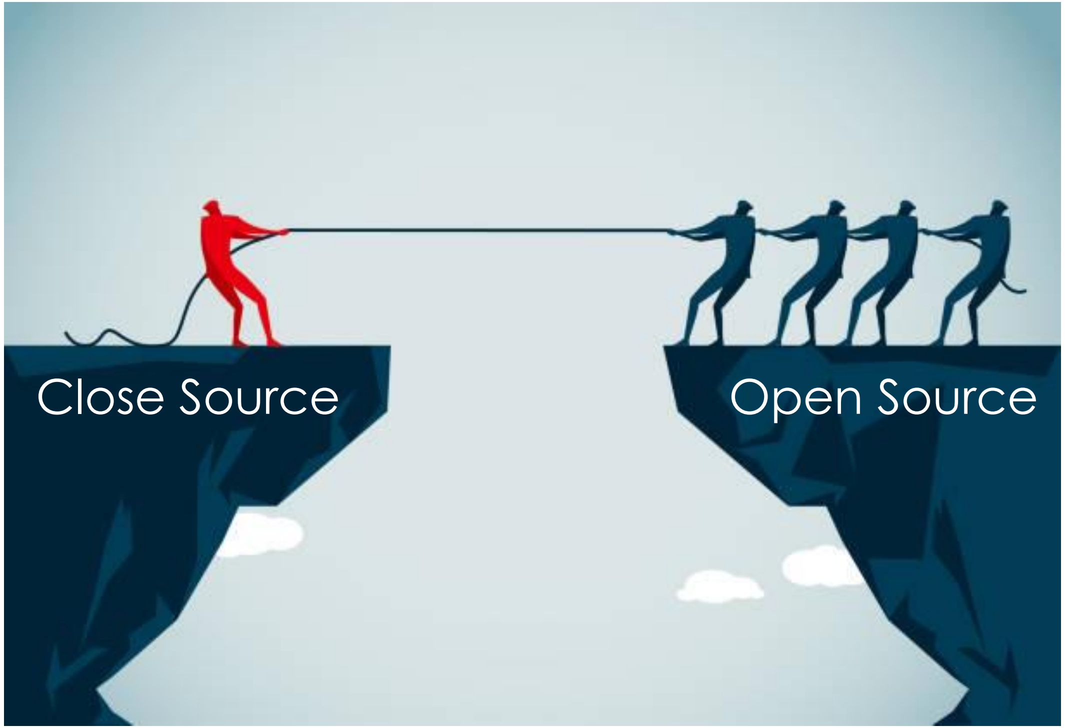
Resource sharing

Verification:
Testbench, tests

Easy communication
No NDA, permissive license

Contribution gifts

Unfair competition



- ✓ **Develop faster**
- ✓ **Increase quality and performance**
- ✓ **Provide great recognition for workers**

Repository

GitHub

https://github.com/openhwgroup/cva6

What are the challenges of Open-Source ?

- Code integrity and quality
- Confidentiality
- Controllability

Code integrity and quality

Bugs
Trojans

Create a more performant industrial product

Solutions

- ✓ Code review
- ✓ Code & Functional coverage
- ✓ Continuous integration

Confidentiality

Threats:
- Code is public
- Open-Source introduces new threats

Needs:
- Protect our industrial IPs
- Produce secure products
- Be eligible to certifications

Solutions

- ✓ Vulnerability study
- ✓ Design differentiation
- ✓ Product is composed of Open Source and Thales assets

Controllability

Threats:
- Exportation rights
- A few information about committer origin
- Roadmap choices

Needs:
- To remain master of our choices
- To be able to exploit the code

Solutions

- ✓ Leading Open-Source working groups
- ✓ Being committer
- ✓ Strong European footprint to enable sovereignty

Thales combines the best of the two worlds

OpenHW Group – CVA6

Verification plans and Tests
Review quality
Up-to-date features

Thales internal assets

Security
Domain-specific acceleration
Industrialization

Expanding open-source hardware

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RISC-V student contest

> Organized by

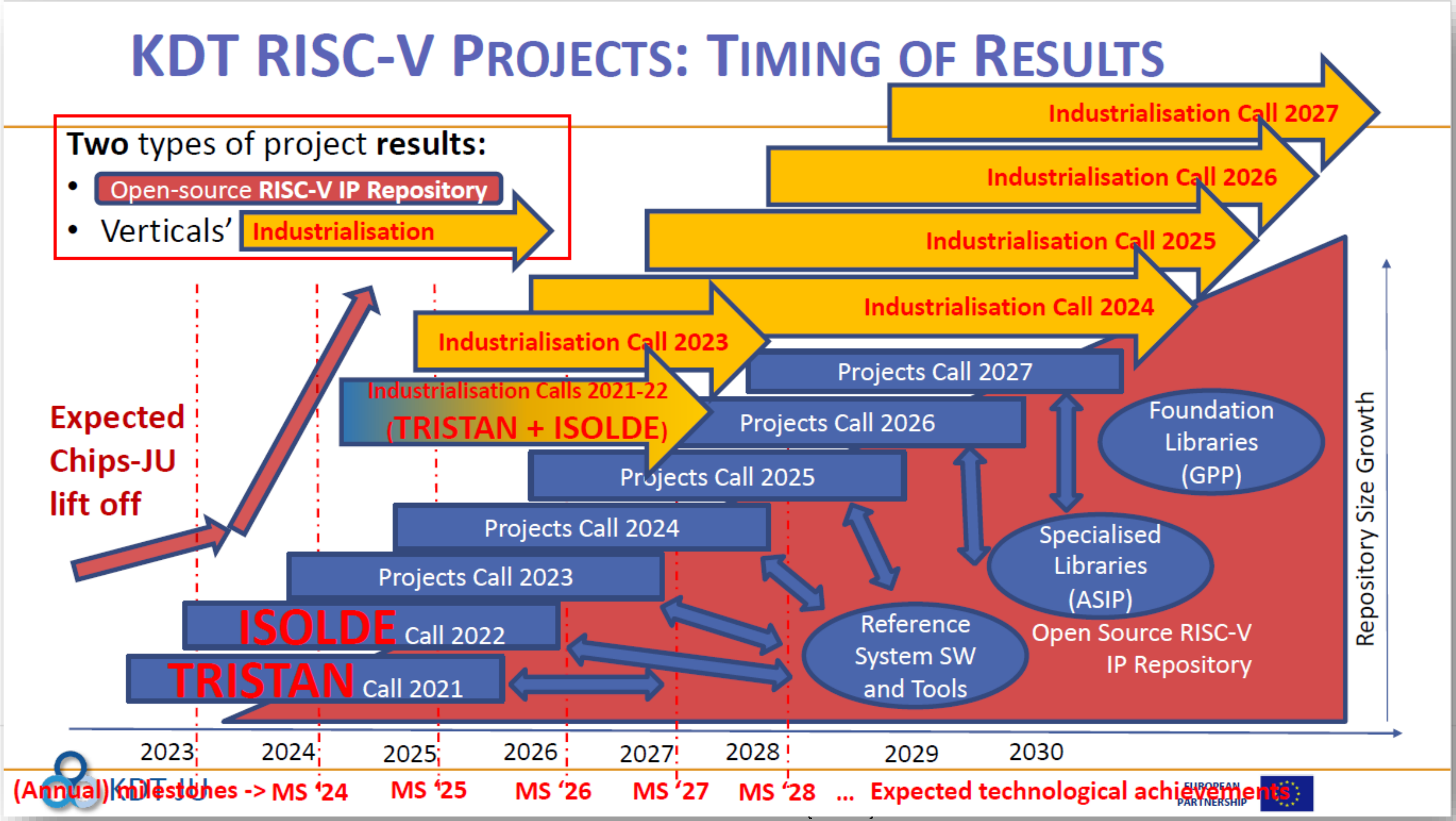
> Objectives

- Promote RISC-V and computer architecture in French education
- Extend RISC-V and OpenHW communities
- Strengthen industry-academy connections

> 4 editions

- 2020-2021: Improve CV32A6 FPGA performance
  - 13 teams from 10 universities
  - Awarded: Télécom Paris, U. Toulouse III
- 2021-2022: Improve CV32A6 energy efficiency
  - 12 teams from 7 universities
  - Awarded: U. Strasbourg (2 teams), IMT Atlantique
- 2022-2023: Defeat RIPE attacks on CV32A6 + Zephyr
  - 19 teams from 14 universities
  - Awarded: INSA Toulouse, CentraleSupélec
- 2023-2024: AI acceleration in CV32A6 (ongoing)
  - 13 teams from 11 universities

The EU has an ambitious RISC-V and open-source roadmap



Courtesy Georgi Kuzmanov, Chips JU

Open-source is suited for industrial use

> OpenHW governance
- Not-profit organization steered by its members
- Based on Eclipse Foundation's processes
- Target industrial-grade quality

> Participation is encouraged
- Share IP development costs
- Influence technical content
- Get recognized as a contributor

> Apache / Solderpad permissive licences
- Freely use, modify, integrate in proprietary solutions
- No need to publish modifications, no viral effect

> Value generation
- Share cost instead of purchasing proprietary IP
- Customize for own application
- Increase control on your solutions
- Easier white box certification

> Business models
- Commercial SW/HW/tooling add-ons
- Maintenance and support offers

> Reduced supplier / export risks
- Ability to fork; no end-of-life
- Significantly lower exposition to export control

Acknowledgements

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Thank you

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